Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	44878	sense adj amplifier	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 08:35
L2	48	1 and match adj device	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 08:35
L3	13	1 and matched adj devices	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 08:35
L4	60	2 or 3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 08:35
L5	0	4 and preconditioning adj circuit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 08:36
L6	0	4 and pre-conditioning adj circuit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 08:36
L7	0	4 and pre-condition$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 08:36
L8	8	4 and length near3 time	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 08:42

L9	2	"6038181".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 08:42
L10	2	"6642746".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 08:42
L11	4	9 or 10	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 08:46
L12	6969	preconditioning	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 08:46
L13	1487	12 and sense	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 08:46
L14	373	13 and match	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 08:46
L15	523	13 and match$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 08:47
L16	523	14 or 15	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 08:47

L17	0	16 and match$3 adj device	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 08:47
L18	21	16 and match$3 adj circuit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 09:15
L19	1145	amplifier and precondition$3 and match$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 09:18
L20	679	19 and shift$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 09:23
L21	668	20 and time	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 09:23
L22	364	21 and magnitude	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 09:23
L23	103570	lifetime	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 09:23
L24	58	22 and 23	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 09:25

L25	126021	sense adj amplifier or differential adj amplifier	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 09:26
L26	0	25 and predondition$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 09:26
L27	605	25 and precondition$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 09:26
L28	92	25 and pre-condition$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 09:26
L29	667	27 or 28	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 09:26
L30	189	29 and match	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 09:26
L31	84	30 and shift	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 09:27
L32	52	31 and magnitude	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/06 09:27

US-PAT-NO: 5414663

DOCUMENT-IDENTIFIER: US 5414663 A

TITLE: VLSI memory with an improved sense amplifier with dummy bit lines for modeling addressable bit lines

DATE-ISSUED: May 9, 1995

INVENTOR-INFORMATION:

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Padgett; Clarence W.	Westminster	CA	N/A	N/A
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ASSIGNEE INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
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APPL-NO: 08/071892

DATE FILED: June 3, 1993

PARENT-CASE:

This is a division of application Ser. No. 07/912,112 filed on Jul. 9, 1992 now U.S. Pat. No. 5,241,497.

INT-CL: [06] G11C007/00

US-CL-ISSUED: 365/210, 365/233.5 , 365/189.01

US-CL-CURRENT: 365/210, 257/E27.103 , 365/189.01 , 365/189.05 , 365/195 , 365/203 , 365/230.04 , 365/233.5

FIELD-OF-SEARCH: 365/210; 365/233.5 ; 365/189.01 ; 365/205 ; 365/23.1

REF-CITED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL	
4989182	January 1991	Mochizuki et al.	365/210	N/A

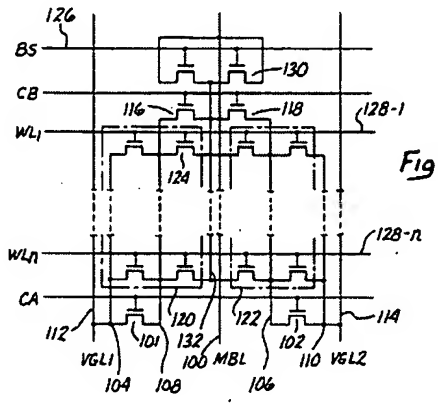
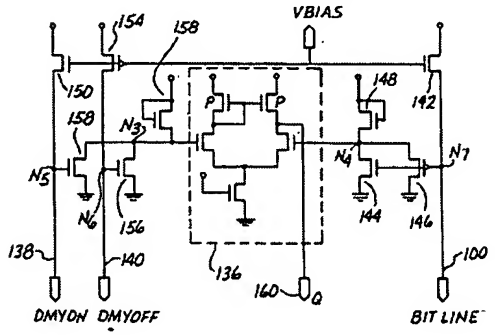


Fig. 9

Fig. 10



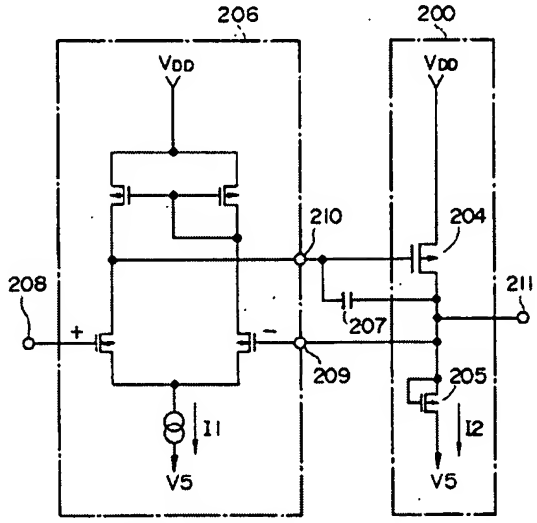
V3, and OP-amps configured as shown in FIG. 10 (hereinafter called n-type OP-amps) are used as the OP-amps that supply V2 and V4.

(45) The voltage divider portion 203 comprises nine transistors connected in series, with each drain region short-circuited to the corresponding gate electrode, and these transistors are used instead of resistors to divide the voltages. In this case, since these transistors are set to all have the same current supply capability, the voltages between V0 and V5 can be accurately divided by nine (1/9 bias). Of the voltages divided into nine in this manner, assume that the first voltage on the low side next to V0 is called V1 and the second voltage is called V2, and the first voltage on the high side next to V5 is called V4 and the second voltage is called V3. The voltage division could, of course, be done using a resistor as shown in the prior art examples of FIG. 33 and FIG. 34. However, in order to try to reduce the demand current, this resistor must have a large resistance, but the use of such a large resistance in an IC causes problems such as a large area is necessary and new fabrication processes must be added. In contrast, instead of large resistances, this embodiment uses transistors in which the drain region and gate electrode are short-circuited. This ensures that the consumption of current flowing though the voltage divider portion 203 can be restrained to the order of 0.2 .mu.A.

(46) A transistor-level circuit diagram of the p-type OP-amp of FIG. 7 is shown in FIG. 8. This p-type OP-amp comprises a differential amplification portion 206 and a drive portion 200. The circuitry of the differential amplification portion 206 has two input terminals, a positive input terminal 208 and a negative input terminal 209 and one output terminal 210, and the manner in which the circuitry amplifies the voltage difference between the two input terminals and outputs it from the output terminal 210 is well known, so further description thereof is omitted. The drive portion 200 has a p-channel drive transistor 204 and an n-channel load transistor 205. Further, a capacitor 207 for preventing oscillation is provided between the differential amplification portion 206 and drive portion 200. The configuration is a voltage-follower connection, in other words, the configuration is such that the negative input terminal 209 of the differential amplification portion 206 is connected to an output terminal 211 of the OP-amp.

(47) The p-channel drive transistor 204 and n-channel load transistor 205 in the drive portion 200 are connected in series, and this connection point is the output terminal 211 of the OP-amp. Connecting the drain region and gate electrode of the n-channel load transistor 205 together makes the transistor function as a resistor. The output terminal 211 of the OP-amp is connected to the negative input terminal 209 of the differential amplification portion 206, and the output terminal 210 of the differential amplification portion 206 is connected to the gate electrode of the p-channel drive transistor 204. Connecting the circuitry in this manner ensures that the voltage applied to the positive input terminal 208 appears at the output terminal 211 remaining the same level. The differential amplification portion 206 ensures that the positive input terminal 208 and the output terminal 211 of the OP-amp are at

FIG. 8



p-TYPE OP-AMP

The trigger circuit can be understood as being comprised of four sections. A first section 300 is an sensing stage which detects the difference between DMYON and DMYOFF as utilized and described in connection with the sense amplifier of FIG. 12.

(70) A second section generally denoted by reference numeral 302 is comprised of three differential amplifier stages used to amplify the sense signal from sensing stage 300. The amplified signal is then coupled from differential amplifier 302 to a level detect stage, generally denoted by reference numeral 304.

(71) Level detect stage 304 converts the output from the last differential amplifier of differential amplifier stage 302 to a full level signal with predetermined rise and fall times with no indeterminate signals in relation to the timing and voltage levels required by the sense amplifier to which TRIG will be supplied. Stage 304 is set to switch at an operating point on the transition of the signal from differential amplifier 302 that is steepest and thereby minimizes indeterminacy that might arise from switching on a more slowly changing portion of the differential amplifier's output.

(72) An inhibit stage, generally denoted by reference numeral 306, is used to prevent false triggering during a nonsensing time period when the precharge signal PC2 is active.

(73) Sensing stage 300 is designed to match the characteristics of the sense amplifier, such as described in connection with FIGS. 10 and 12, as closely as practical and uses the DMYON and DMYOFF signals to determine whether there is enough current in the bit line to latch the data and to turn on the output drivers. This circuit compensates for process variations in the device parameters and for variations in the sizes of the ROM cell arrays.

(74) Consider now in more detail the operation of sensing stage 300. Sensing stage 300 utilizes FET's 308-314 which are constructed so that they are similar in size to the those of the sense amplifier, namely, two transistors 170, 172 and 174 of FIG. 12. In the layout, the corresponding transistors 308-312 in FIG. 24 have the same length as transistors 170, 172, and 174 in FIG. 12. In the illustrated embodiment the width of these transistors are defined by the following seven conditions:

(75) 1. W170=W172=W174

(78) 2. W170+W172=2 W174

(77) 3. W308+W310=W170+W172

(78) 4. W314=W308+dW

(79) 5. W312=W310+dW

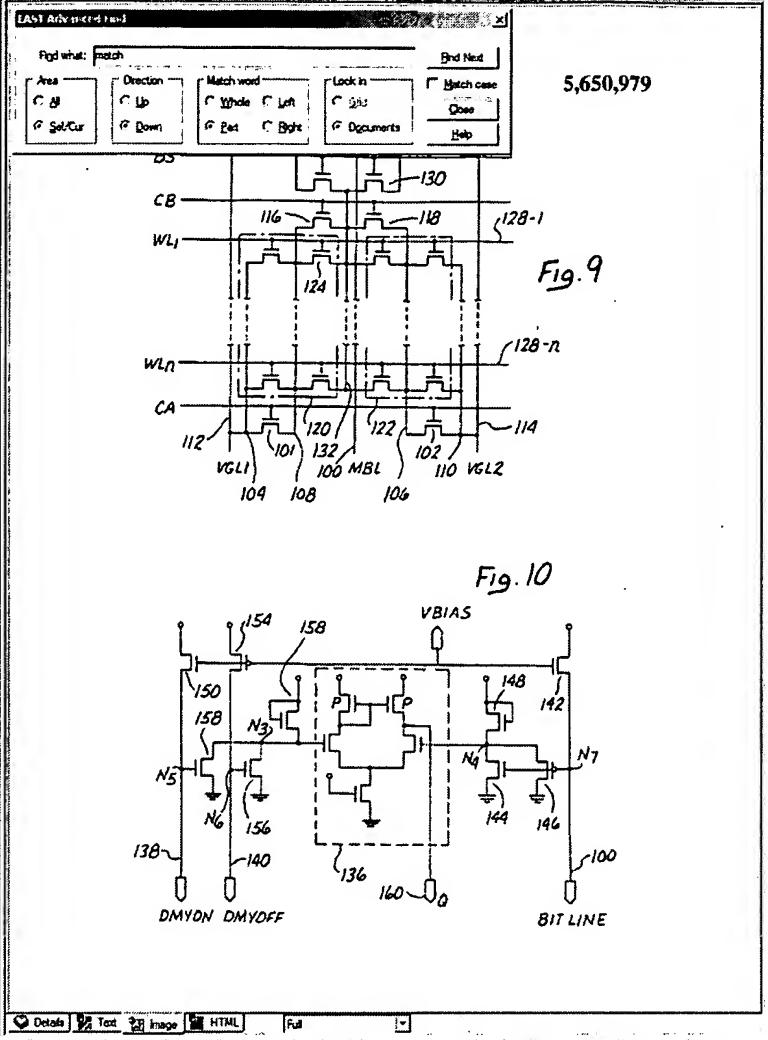


Fig. 9

Fig. 10